General Features

Ceramic Dielectric

Tecdia produces over 95% of the ceramic wafers used to manufacture its capacitors, using fine ceramic powders consisting of unique titanate formulations and proprietary firing processes. A variety of dielectrics are produced from these formulations, covering a range of dielectric constant (K) values, temperature characteristics (TC), and other properties. The products included in this catalog fall within the industry standard dielectric classes I & II. Tecdia also produces EIA class IV single layer ceramic chip capacitors using Grain Boundary Barrier Layer (GBBL) technology.

Electrode Metallization

The sintered wafers are lapped and polished to produce smooth, flat surfaces onto which metal is deposited using dry (sputtering) metallization processes to produce electrodes with ultra-low loss at microwave and millimeter-wave frequencies, and enable reliable thermocompression attachment of gold wires.

<table>
<thead>
<tr>
<th>Metallization Type</th>
<th>Applicable Metals</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion Prevention Layer</td>
<td>TaN</td>
<td>Deposits Ti from diffusion used as resistive material for integrated Resistor-Capacitor and Thin Film Chip Resistor</td>
</tr>
<tr>
<td>Adhesion Layer</td>
<td>TiW or Ti</td>
<td>Create strong bond between metal and ceramic</td>
</tr>
<tr>
<td>Barrier Layer</td>
<td>Pt</td>
<td>Protect adhesion layer during solder attach</td>
</tr>
<tr>
<td>Conductive Layer</td>
<td>Au</td>
<td>Wire bondable, high conductivity layer</td>
</tr>
</tbody>
</table>

Environmental Commitment

Tecdia’s environmental policy is published on our website: www.tecdia.com. Our manufacturing facilities are ISO 14001 certified. All our capacitors are RoHS compliant.
Screening

Tecdia’s capacitors are designed and manufactured for a wide range of applications from high volume commercial communication systems to flight and space programs with stringent quality and performance requirements. The same production processes are used for all our capacitors, whether used for “High Reliability”, industrial or commercial applications. However, selection and screening criteria may vary based on procurement requirements. The screening of capacitors falls within three categories: Standard Grade, Commercial Grade, and Custom.

Regular Scheduled Screening For Single Layer Capacitors

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Quantity Inspected</th>
<th>Allowable Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td>Visual</td>
<td>Inspection Lot AQL II (1%)</td>
<td>Inspection Lot AQL II (1%)</td>
</tr>
<tr>
<td>Capacitance</td>
<td>10 pcs per Wafer Lot¹</td>
<td>0*²</td>
</tr>
<tr>
<td>Electrical</td>
<td>Wire Pull</td>
<td>3 pcs per Wafer Lot</td>
</tr>
<tr>
<td>Dissipation Factor (DF)</td>
<td>Dielectric Withstanding Voltage (DWV)</td>
<td>5 pcs per Wafer Lot*¹</td>
</tr>
<tr>
<td>Insulation Resistance (IR)</td>
<td>High Temperature</td>
<td>3 pcs per Wafer Lot</td>
</tr>
<tr>
<td>Dimension Check</td>
<td>Measurement of Capacitor Dimensions</td>
<td>5 pcs per Wafer Lot*²</td>
</tr>
</tbody>
</table>

¹ Inspection Lot AQL II (1%) is applied for Class IV products.
² Not applicable for class IV products.

Test Lab Capabilities

- **Temperature Cycling**: MIL-STD-883 / Method 1010 Cond. A / B / C
- **Thermal Shock**: MIL-STD-202 / Method 107 Cond. A / B / F
- **Voltage Conditioning**: MIL-STD-883 / Method 105 Cond. A / B / C / F
- **Capacitance & DF**: MIL-STD-202 / Method 505
- **IR**: MIL-STD-202 / Method 302
- **DiV**: MIL-STD-202 / Method 301
- **Bond Pull**: MIL-STD-883 / Method 2011 Cond. D
- **Die Shear**: MIL-STD-883 / Method 2019 less than 3 ksi
- **Temperature Coefficient Limits**: EIA-198 / Method 105
- **Immersion**: MIL-STD-202 / Method 104
- **Moisture Resistance**: MIL-STD-202 / Method 106
- **Life**: MIL-STD-202 / Method 108 less than or equal 150 °C
- **Humidity (Steady State)**: MIL-STD-202 / Method 103
- **Constant Acceleration**: MIL-STD-883 / Method 2001 Cond. A / B / C / D / E / F / G / H / Y1
- **Vibration**: MIL-STD-202 / Method 201
- **Vibration, High Frequency**: MIL-STD-202 / Method 204 Cond. A / B / C / D
- **Vibration, Variable Frequency**: MIL-STD-883 / Method 2007 Cond. A

For more information on proper components use, visit our website. Tecdia may, at its discretion, with or without notice and without liability to Tecdia, suspend sales of the products and/or revise product information from that which is published in the Catalog (B-028-2).

Typical Characteristics

**Typical Temperature Characteristics (Class I)**

- K=1,600
- K=2,800
- K=16,000

**Typical Temperature Characteristics (Class II)**

- K=10,000
- K=16,000
- K=20,000

**Typical Temperature Characteristics (Class IV)**

- K=50,000

**Typical Aging Characteristics**

**Typical DC Bias Characteristics**

- Class I
  - K=1,600
  - K=2,800
  - K=16,000 (6 mil-t)
  - K=16,000 (10 mil-t)
  - K=30,000 (6 mil-t)
  - K=30,000 (10 mil-t)
  - K=50,000 (6 mil-t)
  - K=50,000 (10 mil-t)

**Typical Resonance Frequency (GHz)**

- Class I
  - K=1,600
  - K=2,800
  - K=5,000 (6 mil-t)
  - K=5,000 (10 mil-t)
  - K=10,000 (6 mil-t)
  - K=10,000 (10 mil-t)
### Single Layer Capacitors Type A

**Class I & Class II**

Class I and II single-layer capacitors with a border on the top electrode to aid with visual recognition and to prevent shorting due to epoxy creep up.

<table>
<thead>
<tr>
<th>Electrode Metallization Scheme</th>
<th>Top: TiW - Au, TaN - TiW - Au</th>
<th>Bottom: TiW - Pt - Au, TaN - TiW - Pt - Au</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>AMS</strong></td>
<td><strong>101</strong></td>
<td><strong>K 2 P</strong></td>
</tr>
</tbody>
</table>

#### Selection Guide

**Capacitance Tolerance Code**

- K: ± 10%
- J: ± 5%
- C: ± 0.25 pF*
- B: ± 0.10 pF*

#### Capacitor Code

- **Single Layer Capacitors Type A**
- **Class I & Class II**
- **Top**: 10 mils (0.25 mm)
- **Bottom**: 6 mils (0.15 mm)

**Dielectric Material Code**

- SKT: Standard (1.5 um Au thickness)
- SK: Legacy (4 um Au thickness)

**Thickness Code**

- ± 0.25
- ± 0.13
- ± 0.10
- ± 0.05
- ± 0.025
- ± 0.0125

**Rated Working Voltage**

- 100 V
- 50 V
- 16 V
- 10 V
- 5 V

**Surface Finish**

- 680: Ti - Pt - Au
- 560: TiW - Au, Ti - TiW - Au

### Class IV

High dielectric constant GIBL capacitors with a border on the top electrode to aid with visual recognition and to prevent shorting due to epoxy creep up.

<table>
<thead>
<tr>
<th>Electrode Metallization Scheme</th>
<th>Top: TiN - Au, Ti - TiW - Au</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Class IV</strong></td>
<td></td>
</tr>
</tbody>
</table>

#### Selection Guide

**Capacitance Tolerance Code**

- V: - 0% / + 100%
- M: ± 20%
- K: ± 10%
- J: ± 5%

**Capacitor Code**

- **Single Layer Capacitors Type A**
- **Class I & Class II**
- **Top**: 10 mils (0.25 mm)
- **Bottom**: 6 mils (0.15 mm)

**Dielectric Material Code**

- SKT: Standard (1.5 um Au thickness)
- SK: Legacy (4 um Au thickness)

**Thickness Code**

- ± 0.25
- ± 0.13
- ± 0.10
- ± 0.05
- ± 0.025
- ± 0.0125

**Rated Working Voltage**

- 100 V
- 50 V
- 16 V
- 10 V
- 5 V

**Surface Finish**

- 680: Ti - Pt - Au
- 560: TiW - Au, Ti - TiW - Au

**Note**: Manufactured to metric dimensions. Imperial units are for reference only.
Single Layer Capacitors Type B

Class I & Class II

Class I and II single layer capacitors with borders on top and bottom electrode to aid with visual recognition, preventing shorting due to epoxy creep up, and possessing top-bottom symmetry.

Electrode Metalization Scheme

<table>
<thead>
<tr>
<th>Top</th>
<th>TiW - Au, TaN - TiW - Au</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottom</td>
<td>TiW - Au, TaN - TiW - Au</td>
</tr>
</tbody>
</table>

Capacitance Tolerance Code

- A: ± 0.05 pF*
- B: ± 0.10 pF*
- C: ± 0.25 pF*
- J: ± 5%
- K: ± 10%
- M: ± 20%
- V: ± 0% / + 100%
- Z: ± 20% / + 80%

*Capacitance under 1.0 pF

BMS 101 K 2 P

Cap Code

- C: 12 × 12, 0.30 × 0.30
- F: 16 × 16, 0.40 × 0.40
- H: 20 × 20, 0.50 × 0.50
- K: 24 × 24, 0.60 × 0.60
- P: 31 × 31, 0.8 × 0.8
- R: 40 × 40, 1.00 × 1.00
- S: 50 × 50, 1.25 × 1.25
- T: 60 × 60, 1.50 × 1.50

Size Code

- K5: 0.5
- K10: 1.0
- K15: 1.5
- K20: 2.0

Dielectric Class

- 1: Class I (K = 40 - 280)
- 2: Class II (K = 1,600 - 2,800)

Note: Manufactured to metric dimensions. Imperial units are for reference only.

Application Notes

Tecdia’s SLCs are used in a variety of devices in the optical and RF market including, but not limited to:

- Microwave/Optical Transceivers
- Synthesizers, Oscillators and other signal generators
- TOSA/ROSA/BOSA (Transmit/Receive/Bidirectional Optical Sub-Assemblies)
- Microwave/Optical Amplifiers and Modulators
- High Frequency Signal and RF Measurement Equipment

In these devices SLC function can be summarized into the 3 categories: DC Block, High Frequency Bypass and Impedance Matching.

DC Block

In the DC Block application, the chip capacitor is placed in series in a circuit to prevent the DC bias voltage from one circuit from affecting another. The capacitance is chosen so that the capacitor approximates a short at the frequency of interest.

High Frequency Bypass

In the High Frequency Bypass application, the chip capacitor is placed in shunt (ground) within a circuit to remove high frequency noise or signals by shorting them to ground. The capacitance is chosen such that high frequencies see a low impedance path to ground, while the DC bias voltage or lower frequency signals see a high impedance path to ground and can hence continue along the circuit with minimal attenuation.

Impedance Matching

The Impedance Matching application uses a chip capacitor to provide a specific reactance in a circuit to achieve the desired impedance. These capacitors can be used in numerous lumped circuits to minimize reflections and maintain the signal when passing through elements/circuits of different impedances.
**Single Layer Capacitors Type C**

**Class I & Class II**

Class I and II single layer capacitors without border for solderability, top-bottom symmetry, maximum capacitance density and decreased parasitics.

### Selection Guide

<table>
<thead>
<tr>
<th>Size Code</th>
<th>WE</th>
<th>CC</th>
<th>FC</th>
<th>HC</th>
<th>KC</th>
<th>PC</th>
<th>RC</th>
<th>SC</th>
<th>TD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>0.25 × 0.25</td>
<td>10 × 10</td>
<td>0.08</td>
<td>0.28</td>
<td>0.28</td>
<td>0.08</td>
<td>0.30</td>
<td>0.45</td>
<td>0.48</td>
</tr>
<tr>
<td>0.02</td>
<td>0.50 × 0.50</td>
<td>20 × 20</td>
<td>0.08</td>
<td>0.28</td>
<td>0.28</td>
<td>0.08</td>
<td>0.30</td>
<td>0.45</td>
<td>0.48</td>
</tr>
</tbody>
</table>

**Cap Code**
- **A**: ± 0.05 pF*
- **B**: ± 0.10 pF*
- **M**: ± 0.13 pF
- **Z**: - 20% / + 80%
- **V**: - 0% / + 100%

**Capacitor Code**
- **I**: CMS
- **C**: Type
  - **CMS**: 1R0 : 1.0 pF
  - **0R1**: 0.1 pF

**Electrode Metallization Scheme**
- Top: TiW - Pt - Au, TaN - TiW - Pt - Au
- Bottom: TiW - Pt - Au, TaN - TiW - Pt - Au

**Surface Finish**
- K = 1,600 - 2,800
- M = 300 - 4,000

**Thickness**
- **1**: 10 mils (0.25 mm) ± 1 mil
- **2**: 6 mils (0.15 mm) ± 1 mil

**Note:** Manufactured to metric dimensions. Imperial units are for reference only.

---

**Class IV**

Our most popular high dielectric constant GBBL capacitors for high capacitance density, lower cost decoupling/bypass applications.

### Selection Guide

<table>
<thead>
<tr>
<th>Size Code</th>
<th>WE</th>
<th>CC</th>
<th>FC</th>
<th>HC</th>
<th>KC</th>
<th>PC</th>
<th>RC</th>
<th>SC</th>
<th>TD</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>0.25 × 0.25</td>
<td>10 × 10</td>
<td>0.08</td>
<td>0.28</td>
<td>0.28</td>
<td>0.08</td>
<td>0.30</td>
<td>0.45</td>
<td>0.48</td>
</tr>
<tr>
<td>60</td>
<td>0.50 × 0.50</td>
<td>20 × 20</td>
<td>0.08</td>
<td>0.28</td>
<td>0.28</td>
<td>0.08</td>
<td>0.30</td>
<td>0.45</td>
<td>0.48</td>
</tr>
</tbody>
</table>

**Cap Code**
- **A**: ± 0.05 pF*
- **B**: ± 0.10 pF*
- **M**: ± 0.13 pF
- **Z**: - 20% / + 80%
- **V**: - 0% / + 100%

**Capacitor Code**
- **I**: SKT
- **C**: Type
  - **SKT**: 102 : 1,000 pF
  - **101**: 100 pF
  - **100**: 10 pF
  - **10**: 1 pF

**Electrode Metallization Scheme**
- Top: TiW - Pt - Au, TaN - TiW - Pt - Au
- Bottom: TiW - Pt - Au

**Surface Finish**
- K = 50,000
- M = 80,000

**Thickness**
- **1**: 10 mils (0.25 mm) ± 1 mil
- **2**: 6 mils (0.15 mm) ± 1 mil

**Note:** Manufactured to metric dimensions. Imperial units are for reference only.
Note 1: Manufactured to metric dimensions; Imperial units are for reference only.

Note 2: Typical resonance frequency on page 4 does not apply to this product line.

If you have custom specifications you wish to satisfy then Tecdia can tailor the dimensions, dielectric constant, capacitance, TC and other options to match any particular form factor you are using.

AMS100K3010
AMS210K6010
AMS260K6010
AMS120K3010
AMS180K3010
AMS120K3010
AMS140K3010
AMS160K3010
AMS240K6010
AMS300K6010
AMS500K6010

If you have custom specifications you wish to satisfy then Tecdia can tailor the dimensions, dielectric constant, capacitance, TC and other options to match any particular form factor you are using.

Note 1: Manufactured to metric dimensions; Imperial units are for reference only.

Note 2: Typical resonance frequency on page 4 does not apply to this product line.

If you have custom specifications you wish to satisfy then Tecdia can tailor the dimensions, dielectric constant, capacitance, TC and other options to match any particular form factor you are using.

Note 1: Manufactured to metric dimensions; Imperial units are for reference only.

Note 2: Typical resonance frequency on page 4 does not apply to this product line.
Row Capacitors

An array of 2 or more Type A capacitors onto a single chip for increased capacitance density, fewer components to place and optimal packing efficiency.

**Electrode Metallization Scheme**

<table>
<thead>
<tr>
<th>Top</th>
<th>Bottom</th>
</tr>
</thead>
<tbody>
<tr>
<td>T/R - Ti - Au</td>
<td>T/R - Ti - Au</td>
</tr>
</tbody>
</table>

**Select Guide**

Thickness: 6 mils ± 1 mil (0.15 mm ± 0.025 mm)

<table>
<thead>
<tr>
<th>Size Code</th>
<th>2 Pads</th>
<th>3 Pads</th>
<th>4 Pads</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>20 x 10</td>
<td>20 x 15</td>
<td>20 x 10</td>
</tr>
<tr>
<td>D1</td>
<td>20 x 15</td>
<td>20 x 16</td>
<td>20 x 16</td>
</tr>
<tr>
<td>D2</td>
<td>20 x 20</td>
<td>20 x 26</td>
<td>20 x 26</td>
</tr>
<tr>
<td>D3</td>
<td>50 x 26</td>
<td>50 x 30</td>
<td>50 x 30</td>
</tr>
<tr>
<td>D4</td>
<td>60 x 30</td>
<td>60 x 30</td>
<td>60 x 30</td>
</tr>
</tbody>
</table>

**Cap Code**

- SKT: Standard (1.5 μm Au thickness)
- SKR: Legacy (4 μm Au thickness)

**Resistance Code**

- SKTR: Standard (1.5 μm Au thickness)
- SKR: Legacy (4 μm Au thickness)

**Capacitor Code**

- L4: 4 pads Surface Finish
- L3: 3 pads
- L2: 2 pads

**Cap Tolerance Code**

- A: As Fired
- SK: 0.50 × 0.25
- N: ± 30%
- V: Not Applicable

**Thickness Code**

- 101: 1.00 mm ± 0.25 mm
- 102: 1.50 mm ± 0.25 mm
- 100: ± 40% ± 0.10
- 10: ± 50% ± 0.12
- 100: ± 100% ± 0.15

**Rated Working Voltage**

- 50 V: ± 2.00 × ± 0.50
- 100 V: ± 1.00 × ± 0.50

**Dielectric Material**

- 10: K = 16,000
- 11: K = 30,000
- 16: K = 30,000
- 12: K = 50,000

**Integrated Resistor-Capacitors (IRC™)**

Integration of a resistor onto a capacitor to form a single ceramic chip made with Tecdia's Class IV (K=100,000) dielectric, decreasing BOM count and requiring one less wire bond.

**Electrode Metallization Scheme**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SKTR</td>
<td>SKR</td>
<td>03</td>
<td>± 10 × ± 5</td>
<td>± 13 x ± 5</td>
<td>± 10 × ± 5</td>
</tr>
<tr>
<td>04</td>
<td></td>
<td>± 8 x ± 5</td>
<td>± 13 x ± 5</td>
<td>± 10 × ± 5</td>
<td>± 10 × ± 5</td>
</tr>
<tr>
<td>A</td>
<td>M</td>
<td>± 5 x ± 5</td>
<td>± 13 x ± 5</td>
<td>± 10 × ± 5</td>
<td>± 10 × ± 5</td>
</tr>
</tbody>
</table>

**Cap Code**

- SKTR: Standard (1.5 μm Au thickness)
- SKR: Legacy (4 μm Au thickness)

**Cap Tolerance Code**

- A: ± 10% ± 0.10
- SK: ± 20% ± 0.20
- N: ± 30%
- V: Not Applicable

**Temperature Characteristic of Resistance (TCR)**

- 100 ± 50 ppm / °C ( -10 °C to +85 °C )

**Resistor Rated Power**

- 500 mW @ 70 °C
- 70 mW @ 85 °C
- 70 mW @ 85 °C

**Heat Resistance**

- 125 °C x 5 minutes Ni atmosphere

Note 1: Manufactured to metric dimensions, Imperial units are for reference only.
Note 2: Typical resistance frequency on page 4 does not apply to this product line.
Note 3: Electrical characteristics are measured between top and bottom electrodes only. No bias voltage should be applied between electrodes on top surface.

**Dielectric Material**

- 4: ± 10% ± 0.10
- 10: ± 20% ± 0.20
- 50: ± 50% ± 0.50
Thin Film Chip Resistors

Wire-bondable chip resistors for biasing, RF line termination, and various other applications.

**Resistor Type Code**
- SAW: 1 Resistor
- MBW: 2 Resistors

**Resistance Code**
- 100: $10 \, \Omega$
- 250: $250 \, \Omega$
- 101: $1 \, \Omega$

**Size Code**
- F: 16 x 16 mils (0.4 x 0.4 mm)
- H: 20 x 20 mils (0.5 x 0.5 mm)
- P: 31 x 31 mils (0.8 x 0.8 mm)
- HR: 20 x 40 mils (0.5 x 1.0 mm)

**Thickness Code**
- 2: 10 mils (0.25 mm)

**Rated Power**
- 2A: 100 mW
- 0: No Metallization
- 1: TiW - Pt - Au
- 2: TiW - Pt

**Resistance Tolerance Code**
- J: ± 5%
- K: ± 10%
- M: ± 20%

**Electrode Metallization Scheme**
- TGB: Ti - Pt - Au

**Part Number**
- SAW100K2A21H
- SAW250K2A21F
- SAW250K2A21H
- SAW500K2A21F
- SAW500K2A21H
- SAW500K2A21HR
- SAW500K2A21P
- SAW750K2A21HR
- SAW101K2A21H
- SAW101K2A21HR
- SAW201K2A21H
- SAW102M2A21H
- MBW200K2A21P
- MBW250K2A21P
- MBW500K2A21P
- MBW750K2A21P
- MBW101K2A21P

**Ground Blocks**

Tecdia Ground Blocks are customizable conductive ceramic shims ideal for application within micro-assemblies in both optical and microwave industries.

**Electrode Metallization Scheme**
- Top: Ti - Pt - Au
- Bottom: TiW - Pt - Au

**Part Number**
- TGB025013015
- TGB025025015
- TGB025013025
- TGB025025025
- TGB050013015
- TGB050025015
- TGB050050015
- TGB050013025
- TGB050025025
- TGB050050025

**Size (mils)**
- 10 × 5 × 6
- 10 × 10 × 6
- 10 × 5 × 10
- 10 × 10 × 10
- 20 × 5 × 6
- 20 × 10 × 6
- 20 × 5 × 10
- 20 × 10 × 10

**Size (mm)**
- 0.25 × 0.13 × 0.15
- 0.25 × 0.25 × 0.15
- 0.25 × 0.13 × 0.25
- 0.25 × 0.25 × 0.25
- 0.50 × 0.13 × 0.15
- 0.50 × 0.25 × 0.15
- 0.50 × 0.13 × 0.25
- 0.50 × 0.25 × 0.25

**Custom Part Design Guide**

**Parameter**
- Length: L
- Width: W
- Thickness: t

**Specification**
- Length: 0.25 mm - 2.00 mm
- Width: 0.13 mm - 2.00 mm
- Thickness: 0.08 mm - 0.63 mm
- Resistivity: $3 \times 10^{11} \, \Omega \cdot \text{cm}$ nominal
Thin Film Ceramic Substrates

Tecdia’s Thin Film Substrates technologies combine over 40 years of experience in ceramics, machining, wafer processing, and thin film metallization techniques into one group that specializes in build-to-print thin film metallized ceramic substrates. Features such as fine patterns, electrical wraps, thin film resistors and pre-deposited AuSn are all specialized for miniaturized high-speed communication devices.

- Alumina 99.6% or AlN 170 W/m*K
  - Thickness: 0.1 mm - 3 mm

- TaN Thin Film Resistors

- Electrical Wrap

- AuSn Pre-Deposited Solder Pads

Single Layer Capacitors Options

Predeposited AuSn

AuSn (gold-tin solder) can be added to the metallization stack of any type A (top border only) or type C (no borders) Tecdia capacitors for easier and faster eutectic die attach process.

No Backside Gold

No back side gold capacitors have no Au in the backside metallization stack. The absence of gold helps decrease overall costs, but makes the capacitor only compatible with epoxy attachment.

Packaging

<table>
<thead>
<tr>
<th>Standard Packaging</th>
<th>Material</th>
<th>Color</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Waffle Pack</td>
<td>ABS</td>
<td>White / Natural</td>
<td>2 inch</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Customized Packaging</th>
<th>Material</th>
<th>Color</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Waffle Pack*</td>
<td>Conductive PC</td>
<td>Black</td>
<td>2 inch</td>
</tr>
<tr>
<td>Blue tape (w/Ring)</td>
<td>PVC</td>
<td>Blue</td>
<td>0.6 inch</td>
</tr>
<tr>
<td>Blue tape (w/o Ring)</td>
<td>PVC</td>
<td>Blue</td>
<td>0.67 inch</td>
</tr>
</tbody>
</table>

*Please contact us if you have special requests for the tray pocket sizes.