Thin Film Ceramic Substrate Design Guide

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Section 1: Scope

1.1: Purpose

This document is intended to provide a guide to designers of thin film substrates. The design guide is intended to document the substrate features that can be reliably and economically fabricated in Tecdia's substrate group based in California USA. In many cases, the limits stated herein represent features that have been successfully produced in the past, rather than a fundamental limit on the capabilities of a given process. As more definitive data is obtained on the processes, the procedure will be updated accordingly.

If a designer is able to produce a working design within the limits of this document, one can count on obtaining quality substrates. If the particular needs of a given design fall outside of these limits, the designer should discuss these methods with Tecdia personnel. It may be possible for Tecdia to develop a new process or refine an existing process to achieve the desired results.

1.2: Applicability

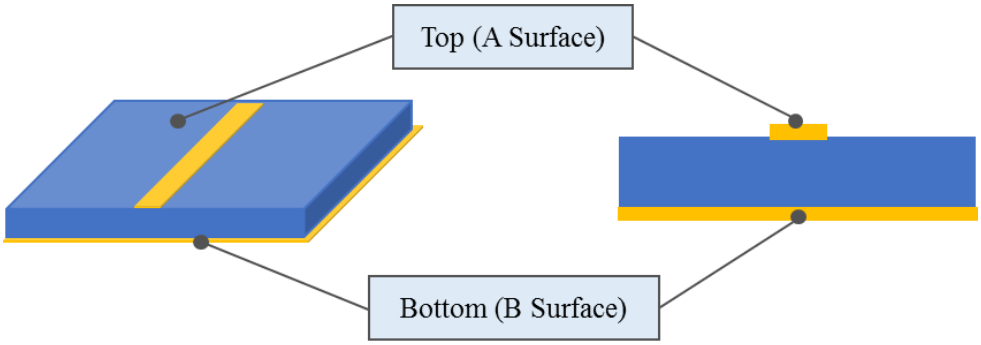
This design guide only applies to thin film ceramic substrates made by the thin film ceramic substrate group based in California USA.

For other capabilities and processes offered at other Tecdia facility refer to "HCT Cebu Design Guide".

Section 2: Introduction to Ceramic Substrates

2.1: Surface Reference

FIG 2.1.1: Surface Reference Methods



2.2: Useful Vocabulary

Substrate: A substance that underlies something, or on which some process occurs, such as a ceramic.

As Fired: A substrate surface condition where the surface receives no treatment after sintering.

Lap and Polish: The processes used to grind and smooth the surface of a substrate after sintering.

Metallization Layer: The layers of metallization applied to the surface of the substrate.

Table 2.2.1: Metallization Stack

Metallization Layer	Applicable Metals	Purpose
Seed Layer/ Adhesion Layer	**Ti/TiW**	Create strong bond between metal and ceramic
Barrier Layer	**Pt/Pd/Ni**	An optional metallization layer that protects covered layers from unwanted embrittlement and diffusion from other metals in the metallization stack. Barrier layers usually sit between the seed layer and the conductor layer or between the conductor layer and the solder layer.
Conductor Layer	**Au**	Wire bondable (Au only), a high current density conductive layer for passing DC and AC current.
Passivation	**Si3N4/Polyimide**	Thin film dielectric layer used for MIM capacitors (Section 9.3), bridges and solder dams

Solder Barrier: A barrier layer placed to prevent diffusion of solder into underlying metallization layer.

Laser Machining: Laser drilling and cutting performed on the ceramic to create holes and cut-outs.

Cut-out: A laser machined feature in the substrate with no metallization on the inside walls.

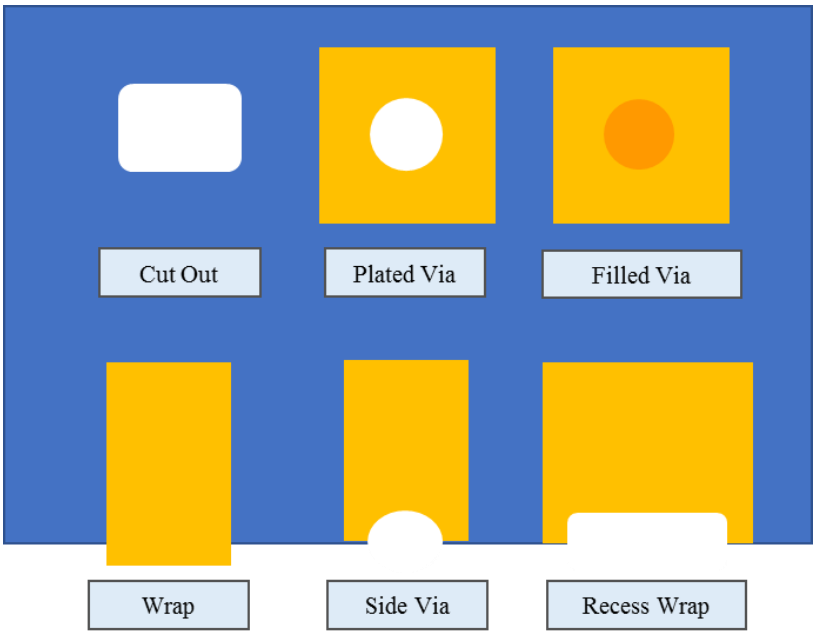
Plated Via: A hole with metallization on the inside walls that creates an electrical connection from the top side to the bottom side of the substrate.

Filled Via: A plated via hole plugged with some material to prevent solder creep up or increase thermal conductivity.

Side Via: A plated via made at the edge of the substrate

Recess Wrap: A wrap made with a recess in the substrate that allows the wrap to be made with a more efficient Post-Cut Laser machining process.

Fig 2.2.1: Wraps and Laser Machined Features



Solder Preforms: Solder pellets placed and reflowed to attach substrates and components

Pre-deposited

AuSn Solder: Solder pads that are applied to components and substrates through various deposition methods such as electroplating, evaporation and sputtering.

Bridge: A raised thin film layer passing over another conductor line separated by a thin layer of air or low ε dielectric.

Solder Dam: A structure created in the circuit to prevent solder from spreading during reflow.

TaN Resistor: Thin Film Resistor structure made from Tantalum Nitride (TaN)

Section 3: Circuit Order Requirements

3.1: Required Information for Quote

Non-CAD files such as PDF, JPEG and GIF can be sent for quoting only. Production/sample requests require CAD files. In order to quote, a drawing with easily recognizable structures and the information in Table 3.1.1, when applicable, must be provided.

Table 3.1.1: Required Information for Quote

Specification	Example
Substrate Material	Alumina (Al_2O_3) 99.6%
Surface Finish	Polished: 0.025 µm Ra Max.
Substrate Thickness with Tolerance	0.254 ±0.025 mm
Chip Size with Tolerance	1±0.05 X 1±0.05 mm
Metallization Stack with Au Thickness and Tolerance	Ti-Pt-Au (1 um Min)
Required Pattern to Pattern Tolerance	± 25 µm
Line and Space Tolerance	± 25 µm
TaN Sheet Resistance	50 Ω/□
Tan Resistor Tolerance	± 20%
AuSn Mixture with Tolerance	Au 80%±10%/Sn 20%±10%
AuSn Thickness with Tolerance	5±2 µm
Via Diameter	0.2 mm
Via/ Cut-Out Location Tolerance	± 50 µm
Via Diameter Tolerance	± 25 µm
Quantity to quote	MOQ, 100 pcs & 500 pcs

3.2: Required CAD File Format

Please consider the following rules when preparing and sending CAD files for Tecdia's substrate group. CAD files are required for mask production.

1. AutoCAD DWG or DXF files only. Other CAD extensions such as Gerber and GDS require conversions that can lead to errors and misinterpretations of the drawing.
2. Please clearly label units used in the CAD file.
3. To create any structure, zero width polylines that create closed polygons are required.

4. Avoid overlapping/double structures or protruding lines, as this will lead to file conversion errors and uncertain interpretation of the CAD design.
5. All drawings must be drawn in a two dimensional (2D). One 2D drawing is preferred for each surface with patterned metallization. Drawing for each surface may be in the same file, but must be clearly labeled.
6. When unclear, metallized areas should be shaded or cross-hatched to indicate where metal is.
7. Data or features that are not part of the thin film design should be removed or placed on a separate, reference only layer.
8. Tolerance for all critical dimensions should be specified within the drawing.
9. Please give each design feature a separate layer. Possible design features include, but are not limited to.
   - Substrate Outline/ Chip Outline
   - Gold Pattern (A, B, C and D Surface on separate layers)
   - Laser machining (Vias and Cut outs)
   - Thin Film Resistors (TaN)
   - AuSn Pre-Deposited Solder
   - Solder Barrier (Pt)
   - Solder Dam (Pt)
   - Bridges
10. For each design feature, please include all required information as explained in each section.

Section 4: Substrate Material

4.1: Material Properties

Alumina (Al_2O_3) and Aluminum Nitride (AlN) are the most common substrate materials processed by Tecdia. Tecdia can also process AlN 200 W/m*K, AlN 230 W/m*K, Al2O3 96%, Glass, Ferrites, Garnates, Sapphire, Fused Silica/Quartz and other hard inert materials. Please inquire for details on materials not detailed below.

Table 4.1.1: Material Properties

Material	Surface Roughness [µ"]	Dissipation Factor at 1MHz	Dielectric Constant (k)	Thermal Conductivity [W/m*K]	Thermal Expansion [µ"/inch/°C)]
As Fired 99.6% Alumina	A Side < 2 B Side < 3	0.0001	9.9±0.1	30	7.1
Polished 99.6% Alumina	< 0.5	0.0001	9.9±0.1	30	7.1
Aluminum Nitride 170	8~24	0.001	8.6	170	4.6
Fused Silica (Quartz)	7	0.0000015	3.8	1	0.55
Polished Sapphire	1	0.0086	11.5	N/A	5.3

4.2: Substrate Thickness Availability

Available wafer sizes and thicknesses for each material are given in Table 4.2.1.

Table 4.2.1: Al_2O_3 and AlN Available Thicknesses

Wafer Size	Standard Thicknesses and Tol	Min and Max
2" x 2" 3.25" x 3.25" 4" diameter 4.5" x 4.5"	0.254 ± 0.025 mm 0.381 ± 0.025 mm 0.635 ± 0.025 mm	Min: 0.1 mm Min Tol: ± 0.0127 mm Max: 2 mm

Wafers thinner than the recommended minimum thickness above can result in substrate warping and cracking. Not all wafer sizes available for thicknesses less than 0.254mm.

Section 5: Conductor Layer

5.1: Metallization layer

Tecdia's standard metal stack is TiW-Au, but Tecdia also offers a range of metals for different environments and attachment conditions. Possible metals and thickness ranges can be found in table 5.1.1 below.

Table 5.1.1: Available Metallization

Layer	Metal	Standard Thickness	Possible Range
Seed Layer	**Ti, TiW**	0.06 µm	0.03 ~ 0.1 µm
Barrier Layer	**Pt, Pd, Ni**	0.15 µm	0.05 ~ 0.3 µm
Conductor	**Au**	1um	0.1 ~ 7 µm

Contact Tecdia regarding metals and thicknesses outside of range given in table.

5.2: Conductor Pattern Tolerances

For all designs as gold increases, maintaining tight tolerances and small features becomes more difficult. Minimum and standard feature limits are given in table 5.2.1.

Fig 5.2.1: Conductor Tolerances on AB Designs

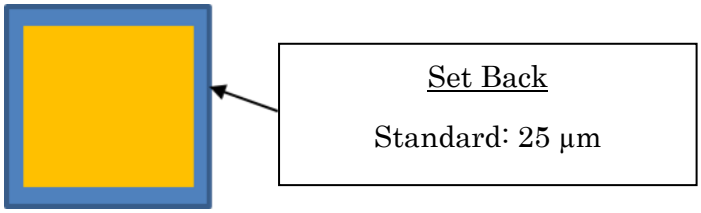
Au Thickness	Minimum Line and Space	Standard Feature Tolerance*	Min Feature Tolerance*
≤2 µm	5 µm	±10% Line Width	±5% Line Width
2~5 µm	10 µm	±20% Line Width	±10% Line Width
>5 µm	20µm	±25% Line Width	±20% Line Width

Contact Tecdia regarding tolerances outside of range given in table.

5.3: Set Backs and Trace to Edge Circuits

During the substrate sawing process, there is a significant possibility that the substrate metallization will peel if the saw goes through a metallized portion of the circuit. Therefore, a metallization setback should be left between the metal trace and the edge of the circuit whenever possible. Fig 5.3.1 gives an example of a metallization set back.

Fig 5.3.1: Standard Set Back



5.4: Other Design Tips

Avoid Acute Angles

In the mask creation process, the patterns are formed on the mask using rectangular flashes of light. Certain patterns, especially acute angles, require numerous flashes to form. This can result in over exposure which creates bleeding in these areas of the mask.

Avoid Circular Structures

Circular and round structures cannot keep tight tolerances when compared to straight features with right angles. To keep processing time and cost down, it's best to avoid circular structures when possible.

Keep Gold Thickness Constant Throughout All Surfaces

Having areas of the electrode where the gold thickness is different requires extra lithography and etching processes. The extra steps and defects that occur during the extra steps add unnecessary cost and so varied gold thickness should be avoided when possible.

Section 6: Resistor Layer

6.1: Available Resistor Layers

The resistors formed at Tecdia are normally formed from Tantalum Nitride (TaN) in one of the standard sheet resistivity layers as described in Table 6.1.1.

Table 6.1.1: Available Resistor Layers

TaN Ω/□ Value
25Ω/sq.
50Ω/sq.
100Ω/sq.

Contact Tecdia regarding Resistor Sheet values outside of range given in table.

6.2: Resistor Design

Resistors must be heat treated in order to be stable over time. Heat treating causes the value of the resistor to increase. Standard heat-treated resistor tolerances are ±10%.

The value of the resistor structure can be calculated by the following formula.

$$R = \frac{L \times Rs}{W}$$

L= Length of Resistor

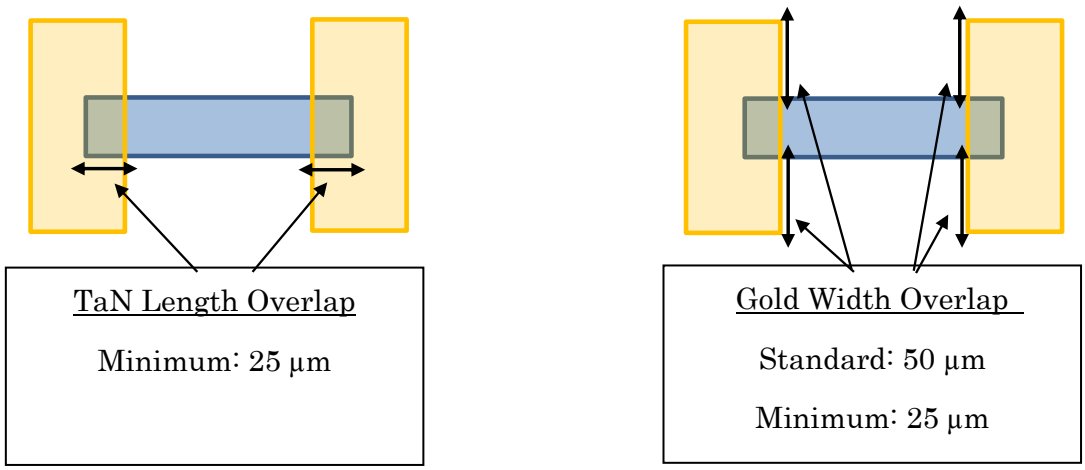
W= Width of Resistor

Rs= Sheet Resistivity (Either 25, 50 or 100 Ω/sq.)

To avoid problems with small misalignment of the gold and resistor patterns, the resistor pattern on the resist mask should overlap the gold pattern and the gold trace be larger than the TaN resistor trace.

Only one resistance sheet can be applied to each surface.

Fig 6.2.1: Gold TaN Overlap Design Rules



Multiple Gold Pads can be placed on top of a single long TaN trace as long as they follow the width and length overlap design rules.

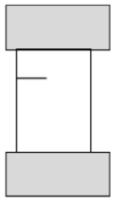
Fig 6.2.2: Multiple Electrode TaN Resistor

Available Resistor Configurations

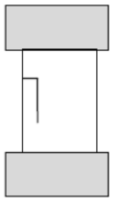
Resistors can be applied to the top, bottom or both surfaces of the substrate. Resistors can be on the substrates that also have any other photo layer (AuSn, solder dam etc.). TaN can be applied to the inside of vias, but the resulting resistance value cannot be easily controlled.

6.3: Laser Trimming

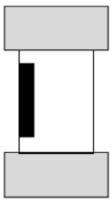
Laser trimming is a process that cuts into the completed resistor in order to precisely adjust the resistors resistance value. There are four types of laser trimming patterns that can be specified: plunge, L, edge-trim and center trim.



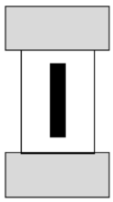
Plunge Cut: This cut is the quickest and easiest and therefore the cheapest cut for the laser system to make. Accuracy of 1% is achievable. The maximum allowable cut is 50% of the resistor width. This can seriously affect the power handling capability of the resistor. Also, it does not result in a good RF match. This type of cut is best suited for reasonably high accuracy DC resistors with plenty of excess power handling ability.



L Cut: This cut is similar to the plunge cut but allows for higher accuracy. It is a little more expensive than the plunge cut. Accuracy of 0.1% is achievable. The first part of the cut is a plunge cut where the value of the resistor changes very quickly and then to fine tune the resistance value the second half of the cut keeps its path along the length of the resistor.



Edge Trim: This cut is made by trimming very slowly on the entire edge of a resistor. It is much more time consuming than the plunge or L cut. Accuracy of 0.1% is achievable. RF performance is better than either the Plunge or L cut. This type of cut is best for very high accuracy DC resistors with more marginal power handling capability or RF resistors with moderate performance.



Center Trim: This cut is made by slowly trimming from the center of a resistor. It is the most time consuming and therefore the most expensive cut available. This cut generally results in much less narrowing of the resistor than the first two cuts which means the power handling of the resistor is less compromised. This type of cut will give the best RF performance of any of the cuts and is therefore recommended for high performance RF resistors.

As laser trimming is time consuming and therefore expensive, it is often desirable to have critical resistors laser trimmed to tight tolerances while leaving the rest of the resistors untrimmed. In order for both types of resistors to achieve design values the process must be adjusted slightly.

1. Design non-trimmed resistors for 100% of the nominal sheet resistivity.
2. Resistive layer sitting under gold pad can add 0.5Ω~1Ω of resistance that should be considered in the design.
3. Add a test resistor also designed to 100% of the nominal sheet resistivity

4. Adjust laser trimmed resistors by reducing size (lowering resistance value) to 90% of the target resistance to accommodate the subsequent laser trim process.
5. After etching, the substrate will be heat-treated until the test resistor is within 10% of its design value.

6.4: Power Dissipation

No definitive studies have been performed to test the long-term reliability of the resistors built under this design guide. Instead the below table gives figures that are commonly accepted in the thin film industry. There are a lot of parameters that will affect the power rating. If your circuit has poor heat sinking use the more conservative value, while conversely, circuits with good heat sinks can use the least conservative numbers.

Fig 6.4.1: Power Dissipation by Area

Most Conservative (Mil Spec and Space Applications)	50 Watts per square inch
Typical	400 Watts per square inch
Least Conservative	1200 Watts per square inch

* Above table does not represent Tecdia measured values

Section 7: Pre-Deposited Solder Layer

7.1: Available Solder Layers

Pre-Deposited Solder Pads are formed from AuSn through an electroplating process with characteristics given in Table 7.1.1.

Table 7.1.1: Plated AuSn Specs

AuSn Ratio	Standard:70/30 Available: 80/20
AuSn Ratio Tolerance	±10%
Thickness Range	2~12 µm (4 µm Standard)
Thickness Tolerance*	± 1µm (3~4 µm) ±2 µm (4.1~7 µm)
Reflow Conditions	300°C in less than 10s

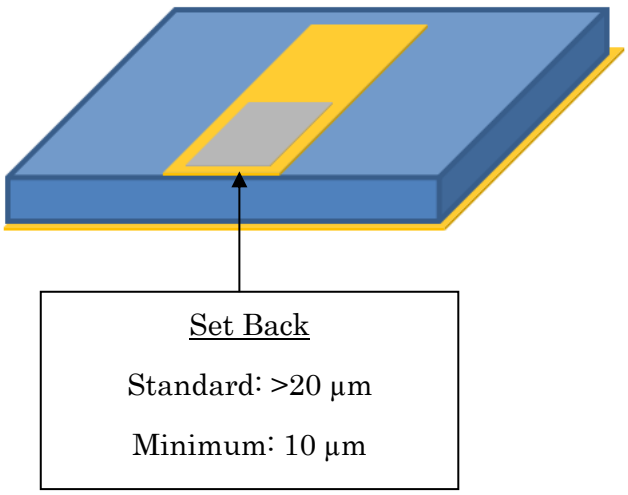
*Due to the difficulty of controlling thickness with plating processes, generally only a minimum thickness requirement is set for AuSn Thickness.

All solder pads must sit on top of a conductor layer.

7.2: Solder Pad Design

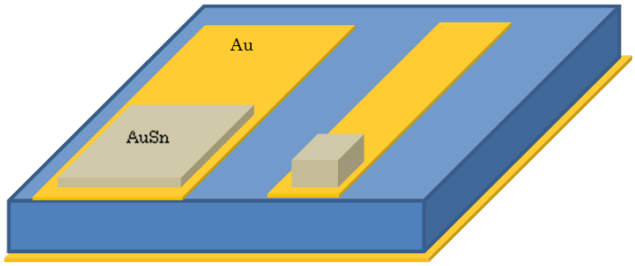
All solder pads sit on top of the conductor layer. To avoid problems with small misalignments between the gold and solder patterns the solder pads need to have a setback as seen in Fig. 7.2.1

Fig 7.2.1: AuSn Gold Set Back



Electroplated AuSn deposits as a function of current and area. When solder pads on the same surface have great variance in area it is very difficult to control the thickness for both pads. In cases where solder pad thickness is critical, electrodes with different areas should be avoided.

Fig 7.2.1: AuSn Gold Set Back



Equal Current and Deposition Time

Available Design Configurations

AuSn Pre-deposited solder can be applied to a single side of any design and any designs with other photo layers. For designs with plated vias, AuSn plating inside the vias is unavoidable and must be acceptable for all drawings with both features on a single substrate.

7.3: AuSn Solder Die Attach General Criteria

a. Preheat components to within 150 to 200°C of the eutectic temperature of the solder pad material before performing die attach.

b. Solder pad should be same dimensions as the bottom electrode of the component, with thickness sufficient to ensure proper attachment.

c. Typically, die-attach processing should be done under an atmosphere of H_2N_2 forming gas, 90 to 95 % N_2 with 5 to 10 % H_2. (Hydrogen serves a reducing agent for thin surface oxides.)

d. With the solder pad in its molten state, quickly place the die on the solder pad and scrub it lightly with tweezers for 2 to 3 seconds.

e. After attaching die, remove the assembly from the die-attaching station and allow it to cool gradually.

f. Solder attach is strongest when performed on fully metalized electrodes containing Pt barrier layer.

g. Tecdia substrates using standard materials and metal stacks can withstand high temperature (400°C) die-attach conditions without physical damage.

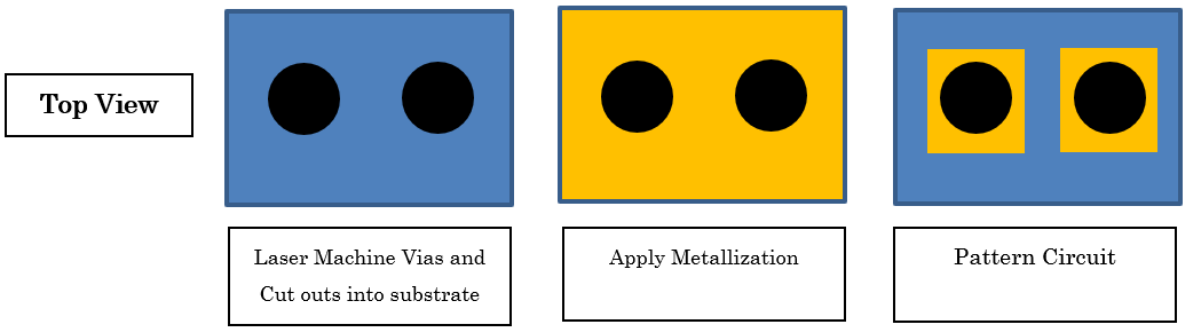
Section 8: Laser Machining

8.1: Pre-Cut and Post-Cut Features

Plated features require pre-cut laser machining while non-metallized features require post-cut laser machining. Plated vias create an electrical connection from the top to the bottom of the substrate.

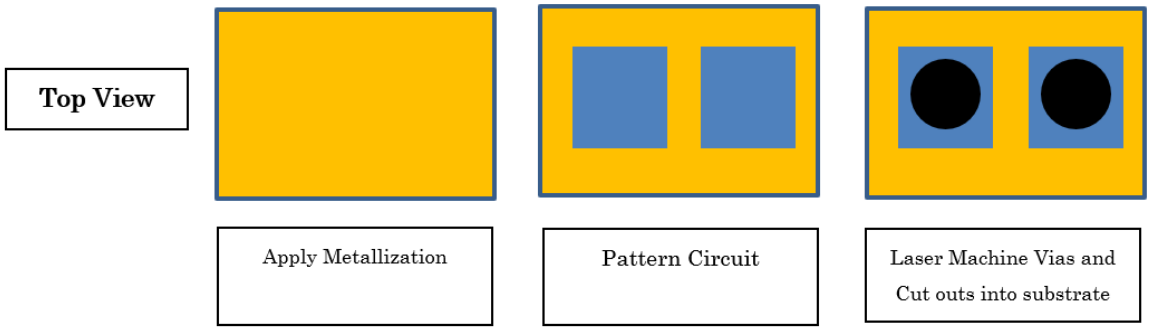
To avoid problems with small misalignments between the gold and vias pre-cut vias and cut-outs require a gold pad to be larger than the via or cut out as seen in Fig 8.1.1.

Fig 8.1.1: Pre-Cut Features



Laser machining through metallized surfaces should be avoided and to avoid possible overlap of the gold pattern with the intended via or cut out area a setback is required as seen in Fig 8.1.2.

Fig 8.1.2: Post Cut Features



8.2: Via and Cut-out Design

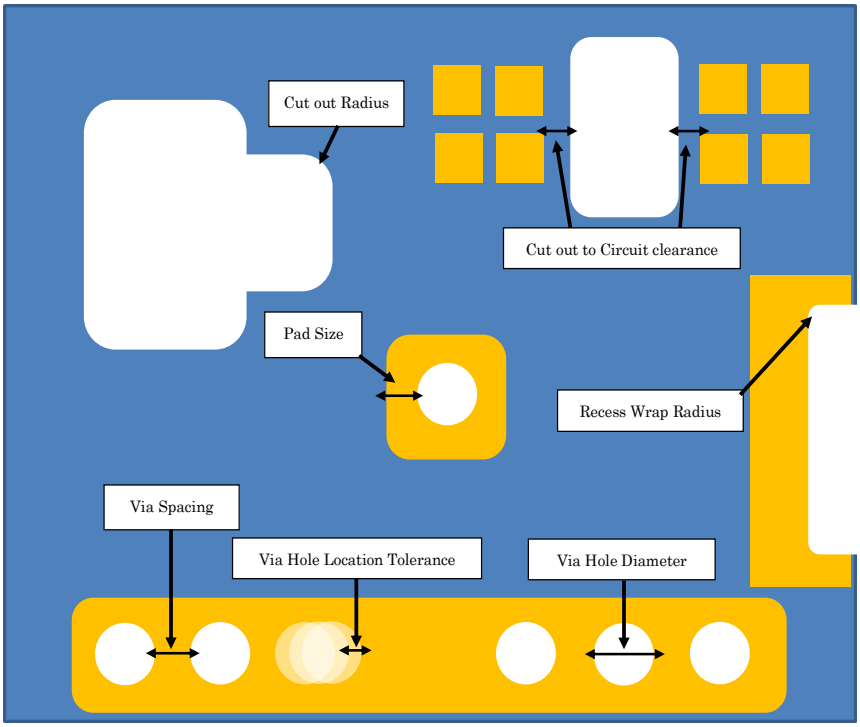
Vias and cut-outs made at Tecdia have the design requirements given in Table 8.1.1. and Fig 8.1.1 below.

Table 8.2.1: Via Parameters

Parameter	Value	Notes
Via Diameter	Whichever is larger, 0.1mm or ¼ of substrate thickness Min	Substrates thicker than 0.381mm require review
Via and Cut-out Location Tolerance	±0.025 mm	
Pad Size	0.1mm Min Distance from Via edge to Gold Pad Edge	Square pads preferred
Distance from Via to Edge	0.25mm Min	Vias too close to edge are prone to cracking
Via Spacing	0.25mm Min	Vias too close together are prone to cracking
Cut-out Radius	0.025 mm Min	Same as Cut-out
Cut-out to Circuit Clearance	0.025 mm Min	

Above values are only estimates subject to change due to varying parameters such as substrate thickness.

Fig 8.2.1: Via Parameters



Distance from Edge of Via to Edge of Substrate
Vias placed near the edge of substrates are prone to cracking. Therefore, leave at least 0.010" or one substrate thickness distance, whichever bigger, between the edge of a via and the edge of the circuit.

Distance between Vias
Vias placed close together are prone to cracking. Therefore, leave at least 0.010" or one time via diameter distance, whichever smaller, between via to via.

8.3: Filled Via

Tecdia has two types of filled vias available

Post-Metallization Filled Via: After completing the circuit conductive epoxy or Polyimide are used to fill the plated vias. The metallized via already creates the connection to the back side so the filled via material does not need to be conductive. This process is easier and cheaper to perform when compared to the Pre-Metallization Filled Via. This process is only useful for preventing solder creep up through the vias.

Pre-Metallization Filled Via: After drilling vias, before applying metals vias are filled with Cu and then the Cu is covered with the thin film metalization stack. This process is more expensive but is useful for increasing thermal conduction at certain areas in the substrate, increasing electrical conductivity of the filled via, creating hermetic seals and preventing solder creep up through the via.

Design Rules Filled Via

1. Filled vias cannot be diced through to create side vias
2. Typically filled vias are only made on 10mil (0.254mm) thick substrates
3. Filled vias require minimum 8mil (0.2mm) diameter vias
4. Filled vias should be one via diameter separated from the chip edge and other vias
5. It is not possible to have filled and non-filled vias on a single design

Section 9: Passivation and Dielectric Layers

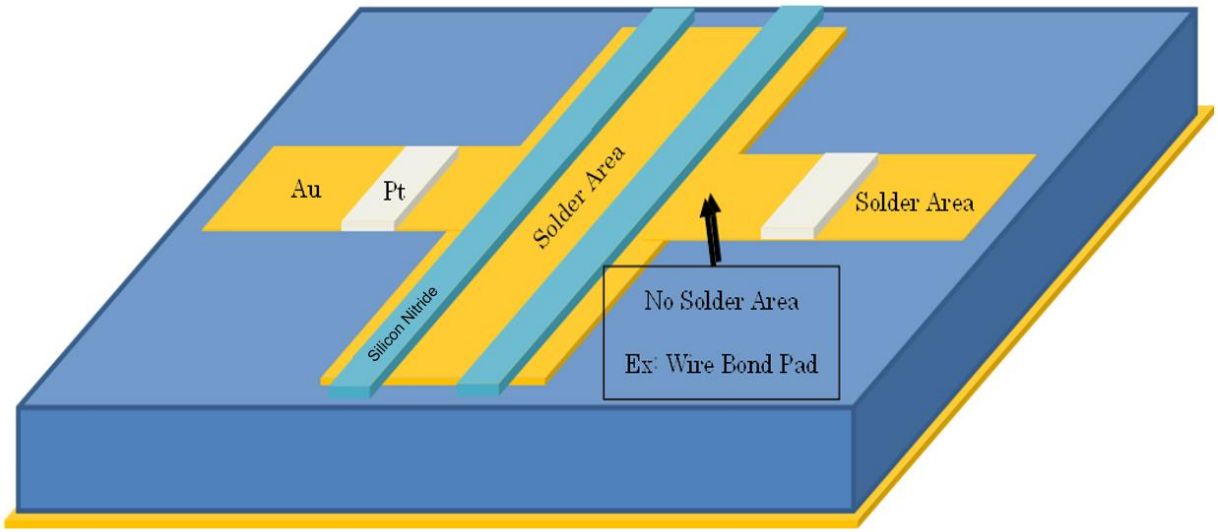
9.1: Solder Dam

Solder Dams are barriers that prevent solder from flowing into unwanted area. There are numerous dielectrics and metals that can be applied to create solder dams. Tecdia Solder dams are normally formed using the materials given in Table 7.4.1 below.

Table 9.1.1: Solder Dam Materials

Solder Dam Material	Recommended Thickness	Notes
Silicon Nitride (Si3N4)	1 µm	Most common and stable dielectric solder dam. Not recommended for high volume
Polyimide	1 µm	Easiest and cheapest dielectric solder barrier when compared with Si3N4
Ti/Cr/TiW	0.5µm	Suitable electrically conductive solder barriers
Pt	0.3µm	Highly heat resistant metal. Cannot be applied thicker than 0.5µm

Fig 9.1.1: Solder Dam Example



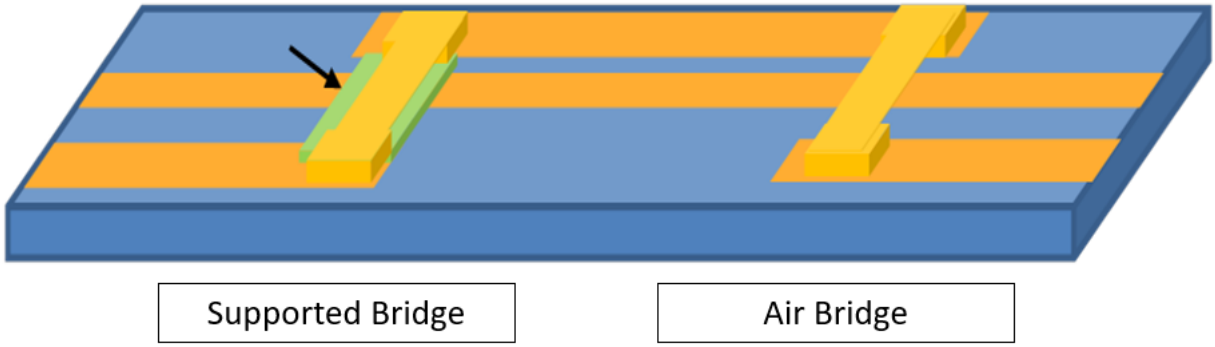
9.2: Bridges

Tecdia offers two types of bridges.

Air Bridge: A bridge created in the conductor layer that allows two traces to cross without connecting. Air Bridges have no dielectric sitting between the overlapping conductors.

Supported Bridge: A bridge created in the conductor layer that allows two traces to cross without connecting. Supported bridges have either Polyimide or Silicon Nitride sitting between the overlapping conductors.

Fig 9.2.1: Bridge Types

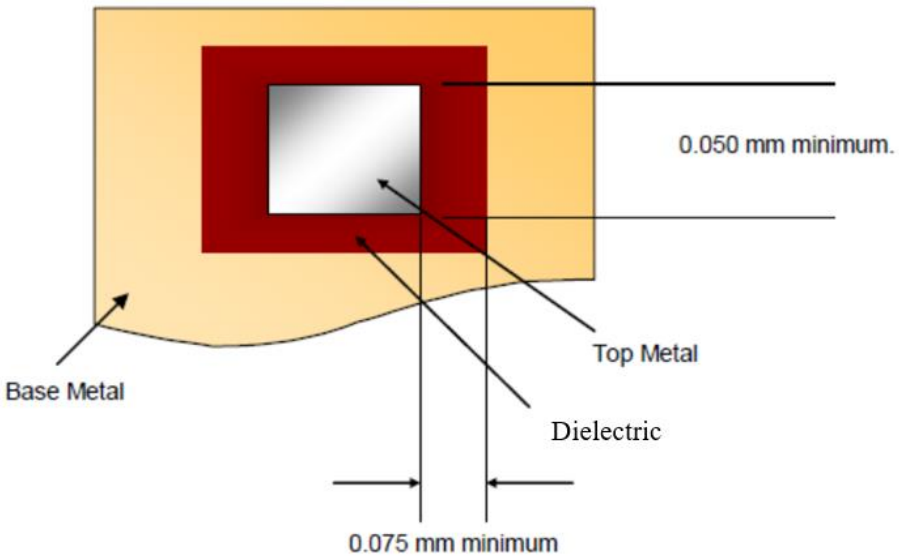


Air bridges are structurally weaker than supported bridges but have improved RF performance compared to supported bridges because of the reduced cross talk between the overlapping traces.

9.3: MIM Capacitors

Through the same processes that allow supported bridges, capacitor elements can be introduced into the substrate circuit. These capacitors are in the pF range and have a breakdown voltage less than 100V depending on dielectric thickness. Image and basic capacitor design rules are given in Fig 9.3.1 below.

Fig 9.3.1: MIM Capacitors



Dielectric options can be found in Table 9.3.1. Silicon Nitride is the preferred material for MIM capacitors.

Table 9.3.1: MIM Capacitor Dielectrics

Dielectric	Available Thickness Range	Dielectric Constant	Breakdown Voltage
Silicon Nitride [Si3N4]	0.5~2 µm	7.5	Breakdown 50V at 1µm
Polyimide	0.5~4 µm	3.3	Estimated based on Textbook Dielectric Strength
BCB	0.5~4 µm	2.6	Estimated based on Textbook Dielectric Strength

Tecdia will only sample test capacitors from each lot unless critical capacitors are specified. With an LCR Tecdia can measure any critical capacitors as required, but please be aware this process is not automated and therefore costly in volume. Silicon Nitride unit capacitance is nominally 50pF/mm2 based on a dielectric constant of 7.5 and a film thickness of 1µm. Expected capacitance can also be estimated using parallel plate capacitor formula.

$$C \approx \frac{\epsilon A}{d}$$

Where,

C= Resulted Capacitance

ε= Dielectric constant of MIM capacitor Dielectric

A= Area of Electrode

d= Thickness of dielectric film

The bottom metal and top metal are generally TiW-Au(2.5µm) where the Au is mostly plated. Connections can be made either by wire bonding or thin film connections.

Fig 9.3.2: MIM Capacitor Connections